WHAT IS CLAIMED IS:

1. A distributed memory test system comprising:

a host computer having one or more test recipes;

plural test sites distributed distal from the host computer, each test site adapted to interface with a memory device under test, each test site having an embedded processor;

a network interfaced with the host computer and the plural test sites, the network communicating the test recipe from the host computer to the embedded processor for execution of the test recipe by the test site.

2. The system of Claim 1 wherein the memory device under test comprises a flash memory device.

3. The system of Claim 1 wherein the memory device under test comprises a fast page DRAM.

4. The system of Claim 1 wherein the memory device under test comprises an EDO DRAM.

5. The system of Claim 1 wherein the memory device under test comprises a SDRAM.

6. The system of Claim 1 wherein the memory device under test comprises a DDR.

7. The system of Claim 1 wherein the memory device under test comprises a rambus.

8. The system of Claim 1 wherein the memory device under test comprises a SRAM.

9. The system of Claim 1 wherein the memory device under test comprises a EEPROM.

10. The system of Claim 1 wherein the network comprises ethernet.

11. The system of Claim 10 wherein the test recipe comprises XML formatted data.

12. The system of Claim 11 wherein each embedded processor accepts the XML formatted recipe data to generate instructions for testing the memory device under test.

13. The system of Claim 1 wherein the network comprises a local area network.

14. The system of Claim 1 wherein the network comprises the internet.

15. The system of Claim 14 wherein the test recipe comprises XML formatted data communicated from the host computer to a test site using TCP/IP.

16. The system of Claim 14 wherein the test recipe comprises XML formatted data communicated from the host computer to a test site using NFS.

17. The system of Claim 1 wherein the test recipe comprises instructions for performing algorithmic testing at the test site.

18. The system of Claim 1 wherein the test recipe comprises instructions for performing vector testing at the test site.

19. The system of Claim 1 further comprising:

plural host computers interfaced with the network, each host computer having one or more test recipes;

wherein each host computer controls tests performed by at least one test site.

20. The system of Claim 19 further comprising a test designer interfaced with the network, the test designer operational to create the test recipes and communicate the test recipes to the host computers.

21. A method for testing memory devices, the method comprising:

communicating a test recipe from a host computer over a network to a test site;

translating the test recipe with a processor at the test site into test instructions; and

testing a memory device at the test site in accordance with the instructions.

22. The method of Claim 21 wherein communicating further comprises sending the test recipe as XML formatted data.

23. The method of Claim 22 wherein the network comprises ethernet.

24. The method of Claim 22 wherein the network comprises a local area network.

25. The method of Claim 22 wherein the network comprises the internet.

26. The method of Claim 22 wherein the network comprises a wide area network.

27. The method of Claim 22 wherein sending the XML formatted data further comprises sending the data using TCP/IP.

28. The method of Claim 22 wherein sending the XML formatted data further comprises sending the data using NFS.

29. The method of Claim 27 wherein the XML formatted data is downloaded from the host to the test site by FTP.

30. The method of Claim 21 wherein translating the test recipe further comprises:

reading the test recipe with a processor at the test site;

associating the recipe with instructions stored at the test site;

executing the associated instructions to generate test data for storage on the memory device;

reading the data from the memory device; and

comparing the read data with a predetermined result to determine whether the memory device accurately stores data.

31. The method of Claim 30 further comprising:

formatting the results from the comparing step into XML formatted data; and

sending the results to the host computer.

32. The method of Claim 30 wherein the executing step comprises executing the instructions with a sequencer at the test site.

33. The method of Claim 30 wherein the instructions generate the test data algorithmically.

34. The method of Claim 33 wherein the instructions call vectors from vector memory stored at the test site.

35. The method of Claim 34 wherein the test data comprises address data and storage data, the address data generated algorithmically and the storage data called from vector memory.

36. The method of Claim 34 wherein the test data comprises address data and storage data, the storage data generated algorithmically and the address data called from vector memory.

37. An apparatus for testing a memory device, the apparatus comprising:

an adapter for physical interfacing with the memory device under test;

a test engine interfaced with the adapter to send test data to the memory device according to test instructions and to read stored data from the memory device for comparison with predetermined results; and

a processor interfaced with the test engine and adapted to interface with a network, the processor operable to receive a test recipe from the network and to translate the test recipe into test instructions for execution by the test engine.